International Journal of Advance Research and Innovation
Vol. 3(1), Jan-Mar 2015, pp. 166-170
Doi: 10.51976/ijari.311530

Article Info
Received: 10 Feb 2015 | Revised Submission: 15 Feb 2015 | Accepted: 28 Feb 2015 | Available Online: 15 Mar 2015

Soft Switching of Phase Shifted Full Bridge DC-DC Converter

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ABSTRACT

Phase shifted full bridge dc-dc converter circuit is presented in this paper. The circuit used for soft switching. Auxiliary cell is connected parallel to the full bridge converter part to achieve softness. The auxiliary cell consist of an active switches, a resonant inductor, a resonant capacitors and coupled winding derived from centre tapped transformer. The auxiliary switches are activated in proper interval to ensure the zero voltage switching to the main switches of converter. The auxiliary circuit create zero voltage switching without any change in voltage/current rating of main switches.

Keywords: *Phase Shifted Full Bridge (PSFB); Zero Current Switching (ZCS); Zero Voltage Switching (ZVS).*

1.0 Introduction

Modern power supplies utilize Switching at high frequency provides better power densities but overall system efficiency reduces because of increased switching losses. The Boost topology is the most popular topology for power factor correction today but it has some disadvantages like very high Electro Magnetic Interference due to reverse recovery of the boost diode and high switching losses caused by hard switching of the boost switch. Many variations of the original boost topology have been suggested to overcome these problems.

The zero voltage transition boost converter is one such solution. In such a converter an auxiliary circuit is employed which is activated only when the boost switch is turning on or off. This auxiliary circuit allows the boost switch to turn on and off under thus reducing the switching losses. However the auxiliary circuit might be very complex and conduction losses in it might offset the expected rise in efficiency. In this thesis a soft-switching boost power converter is proposed. This converter reduces the Electro Magnetic Interference and increases the efficiency because the auxiliary circuit is itself soft-switching and has low conduction losses due to creative placement of the resonant capacitors.

The phase shifted full bridge converter is used for DC-DC conversion in various applications, for example in telecom systems to convert a high voltage bus to an intermediate distribution voltage, typically closer to 48V. The phase shifted full bridge converter is used for DC-DC conversion in various applications, for example in telecom systems to convert a high voltage bus to an intermediate distribution voltage.

This topology allows all the switching devices to switch with zero voltage switching resulting in lower switching losses and an efficient converter. In this work, ZVS for switches in the one leg of the full bridge and zero or low voltage or Switching for switches in the other leg is achieved across the complete load range, by changing dead times for primary side switches based on load conditions.

The gating signals are such that the active switches turn ON at zero voltage by introducing a phase shift between the two legs. The output voltage is a function of the phase shift.

SOFT SWITCHING

- Switching transitions occur under favourable conditions-device voltage or current in zero.
- Reduced switching losses, switch stress, possibly low electromagnetic interference, easier thermal management.
- Must for high frequency operation (also medium at high power levels).

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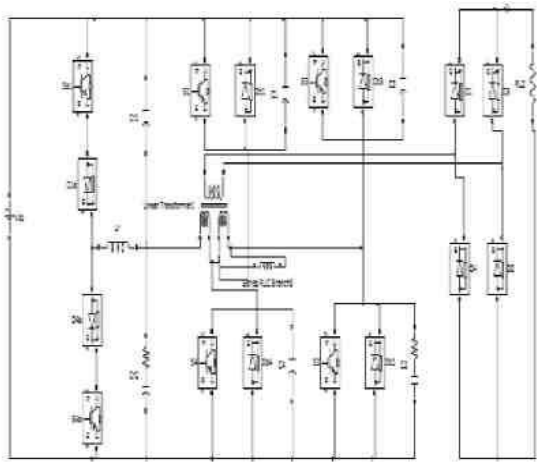
- Usually involves compromises in conduction losses, switching rating, passive components etc.

2.0 PSFB Dc-Dc CONVERTER

The soft switching of PSFB dc-dc converter has an auxiliary cell connected to conventional converter. Auxiliary circuit consists of two active switches S_1a and S_4a two diodes D_1a and D_4a, resonant inductor, resonant capacitors Cr_1 and Cr_4 and coupled winding *LT* derived from the primary winding of the power transformer. S_1 to S_4 is the main switches. DB_1 to DB_4 and C_1 to C_4 are the body diodes and capacitors across the main switches S_1 to S_4 respectively. D_1 to D_4 are the output rectifier diodes of the converter.

Fig 1: Circuit Diagram of Proposed PSFB Dc-Dc Converter



Auxiliary switches S_1a and S_4a are turn ON at zero voltage by introducing a phase shift between the two legs. Gating pulse for the auxiliary switch *S4a* is given, when the main switch *SI* is turned OFF and before S4 is turned ON. Similarly gating to auxiliary switch *S*1*a* is given, when the main switch *S4* is turned OFF and before *SI* is turned ON.

2.1 Operation of proposed system

Interval 0 (t < tO): Prior to positive power transfer, body diode DB1 and S2 are in conduction. Gating SI while DB1 in conduction ensures ZVS during its turn-on.

Interval 1 (t_0 < **t** < t_1): This is a positive power transfer interval. Main switches SI and S2, output rectifier diodes Dl and D2 are in conduction carrying full load current. This interval ends when the gating to main switch S2 is removed.

$$i_m(t-t_0) = i_m(t_0) + \frac{V_{dc}}{L_m}(t-t_0)$$

Interval 2 (t_1 < t < t_2): Rectifier diodes D1 and D2 continue to conduct. Gating S3 while DB3 is in conduction ensures ZVS for S3 during turn-on. S3 is turned ON at ZVS with a delay.

$$i_p(t-t_0) = i'(t-t_0) + i_m(t-t_0) = nI + i_m(t-t_0).$$

Interval 3 (t_2 < t < t_3): This is a freewheeling interval. The main switch S1 and diode DB3 are in conduction. All the output rectifier diodes are in conduction, sharing full load current equally. Interval 3 ends when gating to S1 is removed.

$$i_{D1}(t-t_2) = i_{D3}(t-t_2) = \frac{I}{2}$$

Interval 4 (t_3 < t < t_4): Auxiliary circuit intervals begin when S4a is gated. At the end of this interval, resonant inductor current reaches load current, output rectifier diodes D3 and D4 starts conducting full load current.

$$i_{Lr}(t) = \frac{V_{dc}}{L_r}(t-t_3)$$

Interval 5 (t_4 < t < t_5): Body diode of main switch S4 starts conducting. Gating S4, while DB4 is in conduction ensures ZVS turn-on for the main switch S4.

$$i_{Lr}(t-t_4) = nI + V_{dc}\sqrt{\frac{C_r}{L_r}}\sin(w(t-t_4))$$

Interval 6 (t_5 < t < t_6): Turning S4a OFF ensures ZCS during turn-off for the auxiliary switch. The circuit reverts transition back to power transfer intervals with S3 and S4 ON.

$$i_p = i_m(t_6) - nI$$

Interval 7 (t_6 < t < t_7): This is a negative power transfer Interval. Main switches S3 and S4 and rectifier diodes D3 and D4 are in conduction during this interval.

$$L_m\frac{di_m(t-t_6)}{dt} = v_{ab}(t-t_6) = -V_{dc}$$

Interval 8 (t_7 < t < t_8): Switch S4, diode D3, D4 is in conduction. Gating S2 while DB2 is in conduction ensures ZVS during turn on.

$$i_m(t_2) = i_m^*; i' = nI$$

Interval 9 (t_8 < t < t_9): This is a freewheeling interval. Output rectifier diodes shares the full load current equally during this interval. This interval ends, when gating to main switch S4 is removed.

Interval 10 (t_9 < t < t_{10}): Auxiliary switch S1a and output rectifier diodes D1and D2 conduct the full load current during this interval.

$$i'(t_1) = nI; i_m(t_1) = i_m^*$$

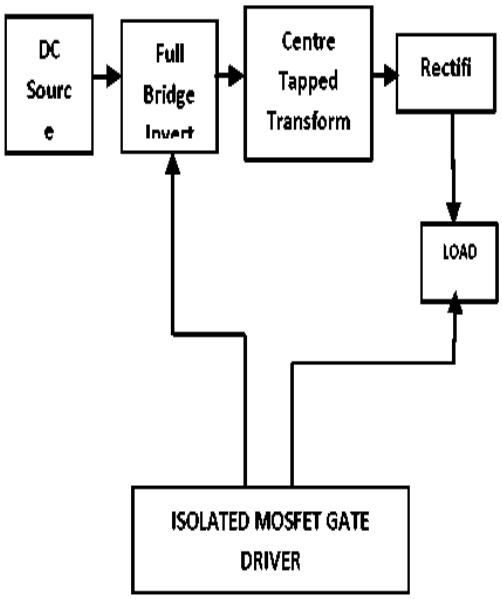
Interval 11 (t_{10} < t < t_{11}): Resonant elements resonate during this interval. Gating S1, when body diode DB1 is in conduction, ensures ZVS turn-on for the main switch S1.

Interval 12 (t_{11} < t < t_{12}): Turning OFF S1a becoming zero ensures ZCS during turn-off for the auxiliary switch S1a .This interval revert back to interval 1, switch S1 and S_2 are in conduction.

$$V_o = nDV_{dc} - IR_d$$

3.0 Block Diagram

Fig 2: Block Diagram of Proposed System



The dc source voltage flows to the full bridge inverter.

The full bridge inverter has four numbers of switches. The proposed circuit connected in parallel to the full bridge inverter section to achieve soft switching.

The inverter is connected to the primary winding of centre tapped transformer.

The centre tapped transformer provides separate output voltages of equal magnitude but opposite in polarity to each other.

The gating sequence for the proposed converter is generated using the gating pulses for the four switches in the inverter are phase shifted between the lagging and the leading legs.

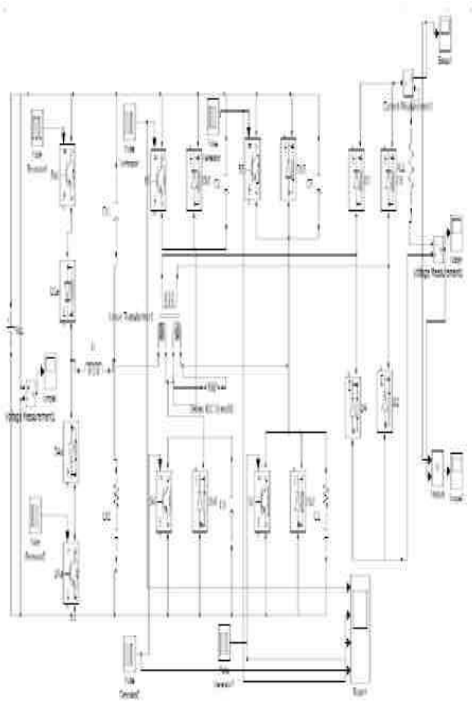
The rectified dc output is derived to the load. A new active soft switching circuit for PSFB is proposed in this paper, which addresses some of the aforementioned problems and maintains the advantage of conventional PWM converters.

The proposed circuit is connected in parallel to the lagging leg as depicted to achieve soft switching.

Novelty in the proposed circuit is the method of generating the voltage required to ensure soft switching for auxiliary switches.

4.0 Simulation Result

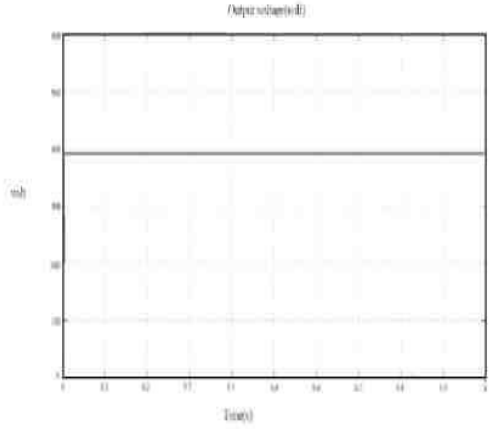
Fig 3: Simulation Diagram



Simulation Results: Circuit simulation waveforms of the proposed active soft-switched PSFB dc-dc converter are shown in Fig. 4.2, 4.3.

1) Gating signals for lagging leg switches (SI and S4) and auxiliary switches (SIa and S4a) is observed that the auxiliary switches (Sla and S4a) conducts for 7% to 10% of total switching period of the converter.
2) Gating signal for lagging leg switch S4 and its drain-to source voltage for 15%, 50%, and 100% load are respectively. It is observed that the active switch S4 is turned ON at zero voltage, from 20% to 100% load variations. The waveforms for 350-W, 100-kHz proposed active soft-switched PSFB dc- dc converter are shown in Figs. 10 and 11 for 20% to 100% load variations. The following are the inferences from these waveforms:
3) Gating signals for lagging leg switches (SI and S4) and auxiliary switches (Sla and S4a) are observed that the auxiliary switches (Sla and S4a) conduct for shorter durations (10% of turn-on time of converter).

Fig 4: Output Voltage



4) Gating signal for auxiliary switch S4a, resonant inductor current, gating signal for active switch S4, and its drain-to-source voltage is observed that the resonant inductor current which is same as auxiliary switch current, rises linearly from zero reducing the turn-on losses in the auxiliary switch. Auxiliary switch current is rested before removing its gating signal. This ensures ZCS for auxiliary switch and diode during its turn-off. Drain-to-source voltage of main switch S4 is zero before it is gated. This ensures ZVS during its turn-on.
5) Gating signal for auxiliary switch S4a , resonant inductor current, gating signal for main switch S4 , and its drain to- source voltage for 20% load are observed that the main switch S4 is turned ON at zero voltage, auxiliary switch is turned OFF at zero current. This is true for the top switch SI also.
6) Gating signal and drain-to-source voltage waveform of leading leg switch S2 for 20% load is observed that the main switch S2 is turned ON at zero voltage.
7) Gating signal for auxiliary switch S4a , resonant inductor current ,gating signal for main switch S4 , and its drain to- source voltage for 50% load are observed that the main switch S4 is turned ON at zero voltage, auxiliary switch is turned OFF at zero current.
8) Gating signal and drain-to-source voltage waveform of leading leg switch S2 for 50% load are observed that the main switch S2 is turned ON at zero voltage.
9) Gating signal for auxiliary switch S4a , resonant inductor current , gating signal for main switch S4 , and itsdrain-to-source voltage for 80% load are observed that the main switch S4 is turned ON at zero voltage, auxiliary switch is turned OFF at zero current.
10) Gating signal and drain-to-source voltage waveform of leading leg switch S2 for 80% load are observed that the main switch S2 is turned ON at zero voltage. It can be summarized from these inferences that the additional auxiliary circuit provides ZVS during turn-on for lagging leg switches SI and S4. The turn-on of leading leg switch S2 and S3 is at zero voltage throughout the load variations. Additional auxiliary circuit provides zero voltage during turn-on for lagging leg switches without disturbing ZVS mechanism for leading leg switches during turn-on.

Fig 5: Output Current

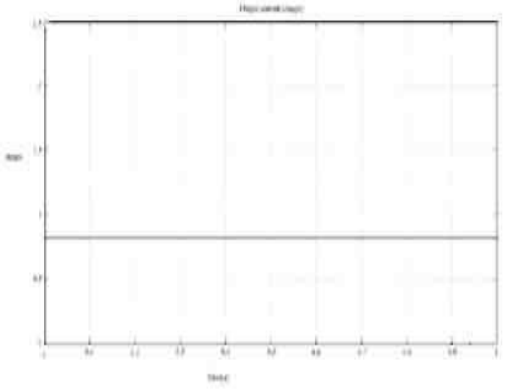
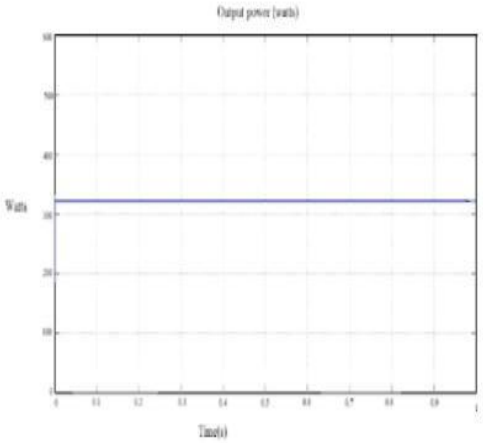


Fig 6: Output Power



5.0 Conclusion

The soft switching of PSFB dc-dc converter is investigated. From the simulation result, it is clear that proposed converter minimize the losses using auxiliary switches. The auxiliary circuit achieves zero voltage during turn-on for main switches without disturbing the zero voltage turn-on conditions for other switches. Thus improvement in the overall efficiency than the conventional converter is presented.

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